**COL 215 – Mini Project**

Yash Malviya 2016CS50403

Hardik Khichi 2016CS50404

CRC Computation

Note: The problem statement for mini project was changed after submission of lab report 3. In accordance to that we had to make some changes to our implementation starting from the scratch. So, many points in this report may not match with the previously submitted reports.

1. Specifications:

The user will enter n (=10) 16-bit binary numbers using the switches on the board. One input is registered after the user presses button no.1. These numbers will be stored one by one in a B-ram cell that can store 10 16-bit vectors.

If the user presses button no.3, a number form B-ram cell will be input to the CRC calculation entity, which will further display the hex value of the calculated checksum.

If the user presses button no.4, a new number will be input to the CRC calculation entity but its 7th-bit will be inverted. Similarly, if user presses button no.5, the number’s 12th-bit will be inverted. Finally, its checksum is displayed.

If the user presses button no.2 (RESET Button), all the numbers in the B-ram cell will be removed. The SSD will start displaying the seed value (i.e. ffff).

1. Overall approach:

We

3)Description of the major subsystems/components and interconnecting signals:

The project contains four major components/entities:

**1) B-RAM component**

addr = To give location to input/output number in B-ram cell.

clk = Clock signal for B-ram cell.

din(16 bit) = Signal for number input.

dout(16 bit) = Signal for number output.

en = Enable(1)/Disable(0) B-ram cell.

we = Write enable.

**2)CRC Calculation unit**

clk= Clock.

pb1 = To load the 16-bit inputs in a B-ram (for n = 10).

pb2 = To reset the CRC calculation, reset the checksum to the seed value.

pb3 = To start the CRC computation with no error introduced.

pb4 = To start the CRC computation with error at the 7th bit.

pb5 = To start the CRC computation with error at the 12th bit.

inp\_bram\_data(16 bit) = Input from input B-ram cell.

crc\_bram\_data(16 bit) = Input from CRC B-ram cell.

data\_inp(16 bit) = Input from switches.

crc\_disp(16 bit) = Calculated CRC to be displayed on SSD from CRC Bram.

wr\_crc(16 bit) = Input for input B-ram cell.

wr\_inp(16 bit) = Input for CRC B-ram cell.

done = Shows if calculation is complete.

resetting = out std\_logic;

started: out std\_logic;

reading: out std\_logic;

-- write enable

we\_inp: out std\_logic\_vector(0 downto 0);

we\_crc: out std\_logic\_vector(0 downto 0);

--addr of brams

addr\_inp: out std\_logic\_vector(3 downto 0);

addr\_crc: out std\_logic\_vector(3 downto 0)

**Port Map Unit**

Validation Methodology